Mechanisms and Temperature Dependence of Single Event Latchup Observed in a CMOS Readout Integrated Circuit from 16-300 K

Cheryl J. Marshall[1], Paul W. Marshall[2], Raymond L. Ladbury[1], Augustyn Waczynski[1], Rajan Arora[3], Roger D. Foltz[1], John D. Cressler[3], Duncan M. Kahle[1], Dakai Chen[4], Gregory S. Delo[6], Nathaniel A. Dodds[5] , Jonathan A. Pellish[1], Emily Kan[1], Nicholas Boehm[6], Robert A. Reed[5], and Kenneth A. LaBel[1]

[1]NASA GSFC,
[2]NASA GSFC Consultant
[3]Georgia Institute of Technology
[4]MEI Technologies, Inc.
[5]Vanderbilt University
[6]Global Science and Technology, NASA-GSFC

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For inquiries: cheryl.j.marshall@nasa.gov

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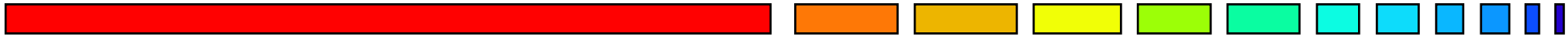
Outline

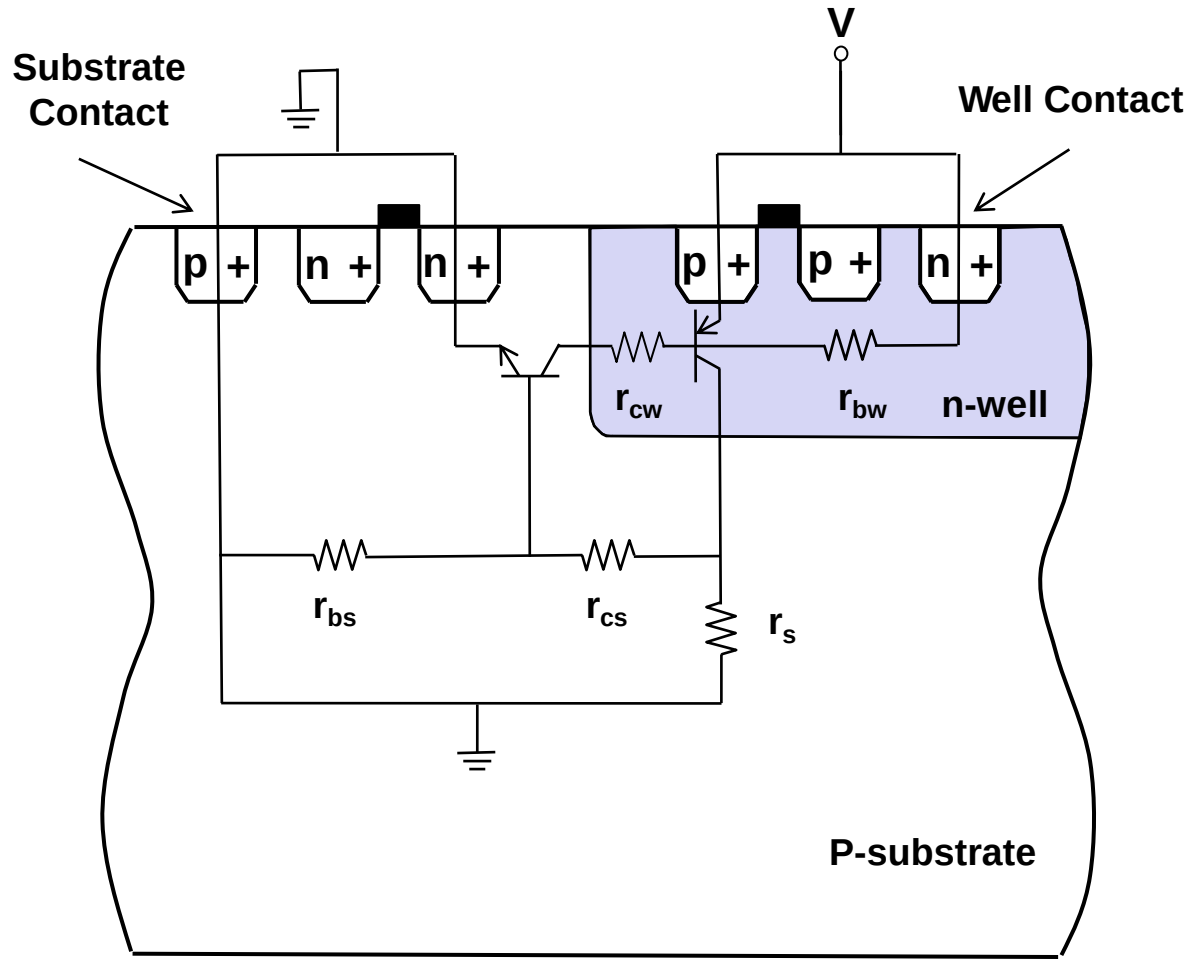


- Review of classical electrical and particle-induced LU in CMOS
- 1st observation of 'anomalous' electrical latchup (LU) from ~4 - 50 K by Deferm *et al.*
- Temperature dependent electrical LU results – 130 nm test structure
- Heavy ion SEL experiment on 0.5 µm ReadOut Integrated Circuit (ROIC)
- Discussion of particle-induced SEL mechanisms at 20 K

Review of Inherent CMOS LU Susceptibility

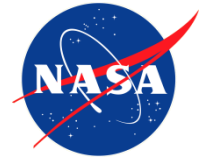
Cross coupled parasitic bipolar transistors inherent to CMOS Technology

- **Current produced by ion strike can forward bias the base emitter junction and begin the SEL sequence**
- **Key device parameters for all temperatures:**
  - **Well & substrate resistivities**
  - **Well & substrate contact proximity**
  - **Minimum n+ - p+, or cathode-anode spacing**



After Johnston, TNS, 1996 & Bruguier and Palau, TNS, 1996

Classical Picture of LU as the Temperature Drops



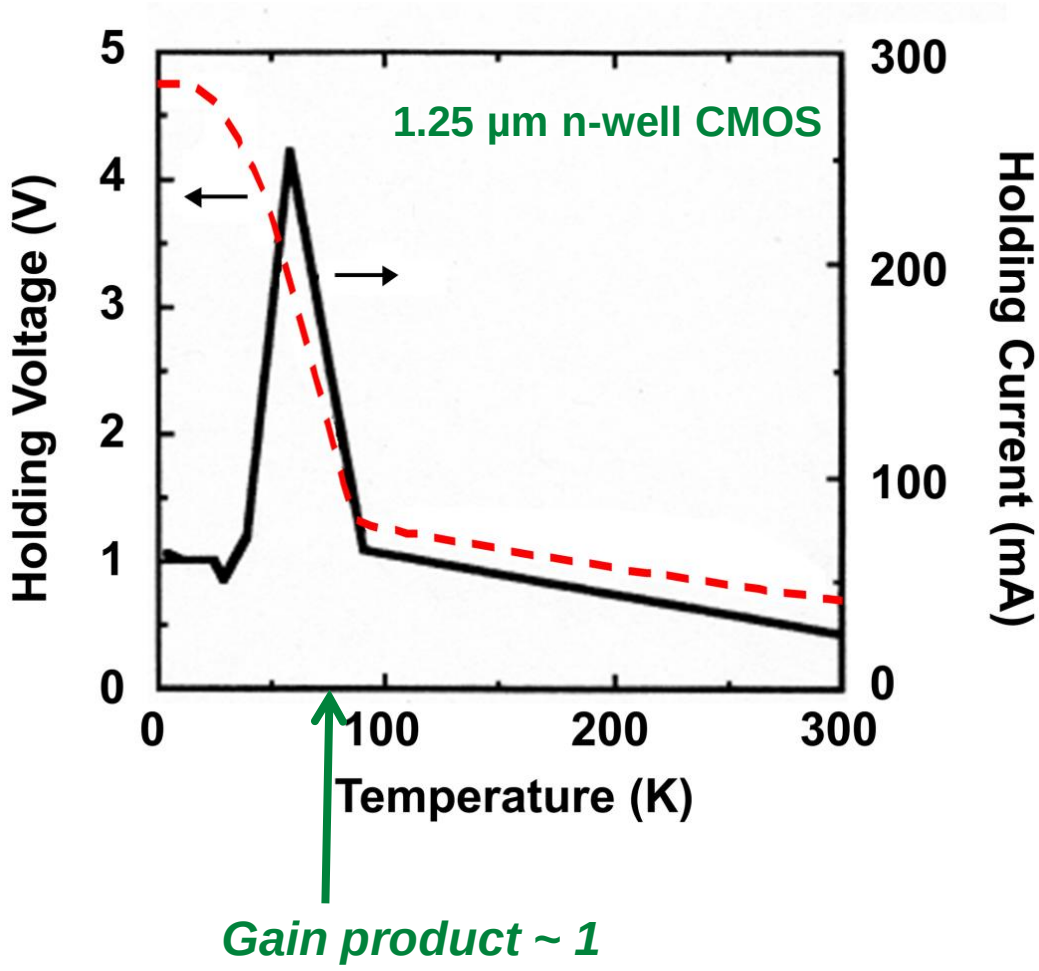
- Electrical and particle-induced LU susceptibilities decrease because:
  - Well & substrate resistances decrease due to increase in mobility and carrier freeze-out.
  - V_{BE} required to support a given collect current increases.
  - Parasitic bipolar gain product is decreasing exponentially with temperature (and also via temperature dependence of the bandgap narrowing in the emitter).
    - Often has little quantitative effect on LU characteristics.
- Below ~75-100 K, regenerative feedback is no longer possible, since $\beta_{npn}\beta_{pnp} < 1$ for the two parasitic BJT common-emitter current gains.

Electrical LU is observed below ~ 50 K

- **Deferm *et al.* suggest shallow-level impact ionization as the source of an exponential increase in free carriers once a threshold field is reached in the internal n- and p- regions of the parasitic pnpn structure, resulting in significant current flow.**
  - **LU condition becomes:**

$$\beta_{npn}\beta_{pnp} > (M_n M_p)^{-1}$$

where M_n & M_p are the shallow level impact ionization coefficients (or rates) for electrons & holes

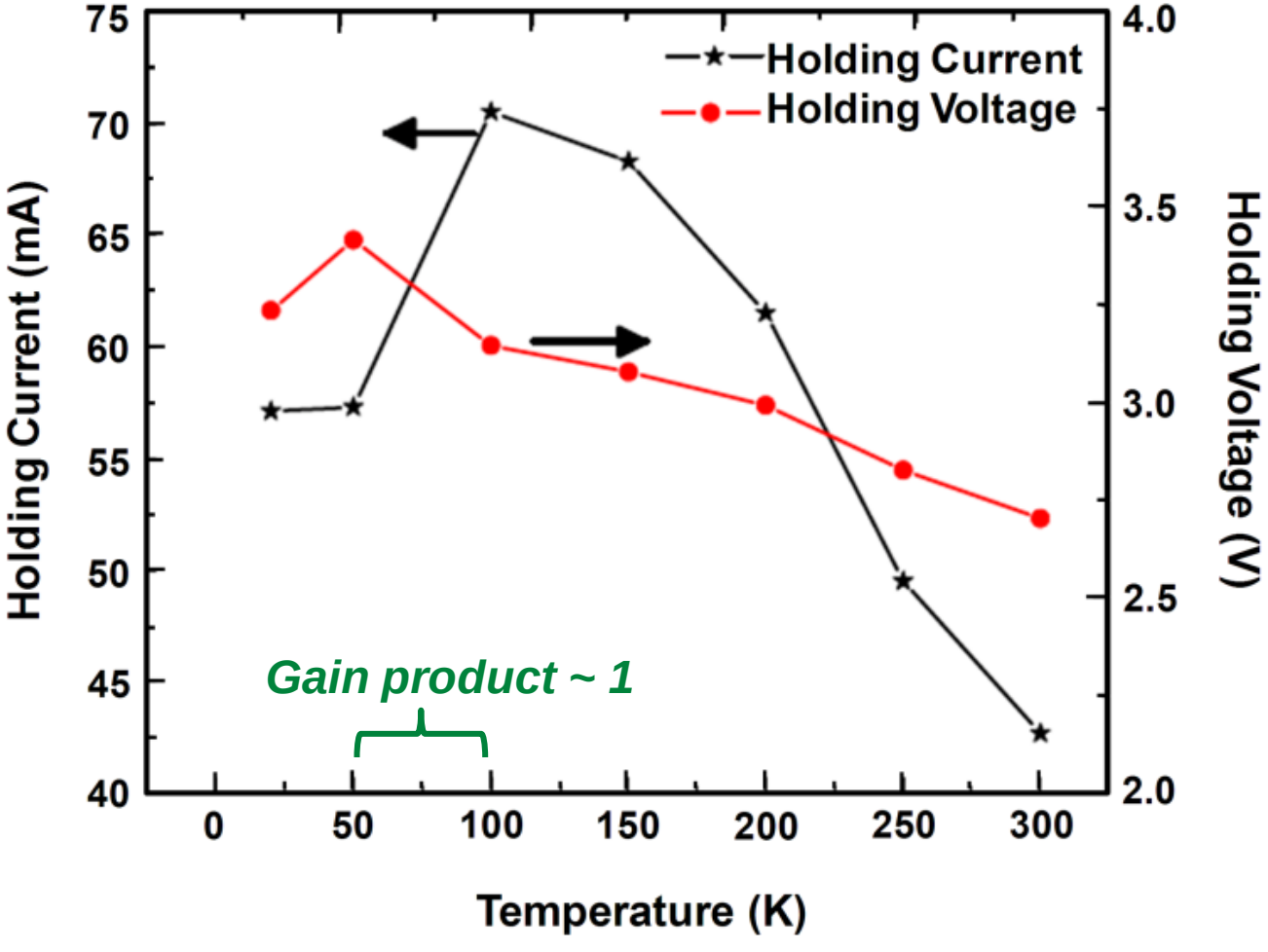


After Deferm et al., Cryogenics 30, 1990.

Temperature Dependence of Key LU Parameters

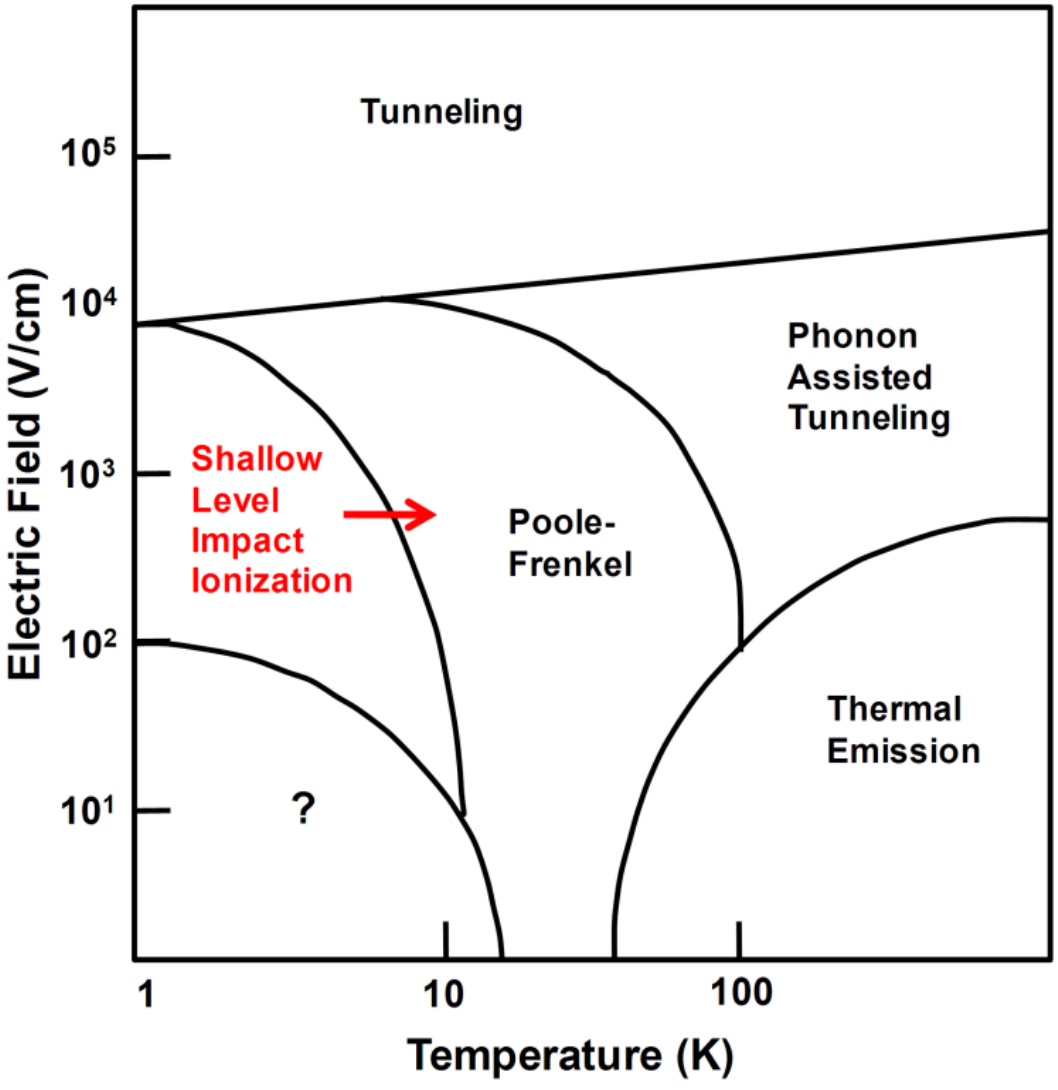
Electrical LU measurements via anode injection

130 nm IBM pnpn test structure



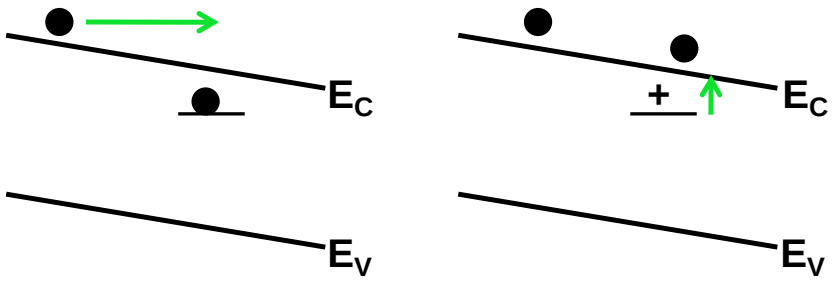
- **Note changes ~50 K where shallow level impact ionization becomes important.**
- **Triggering current and voltages required to initiate LU**
  - **Increase monotonically with decreasing temperature**
- **Vertical pnp gain much larger than for lateral npn**

Dominant Impurity Ionization Mechanisms vs Temperature

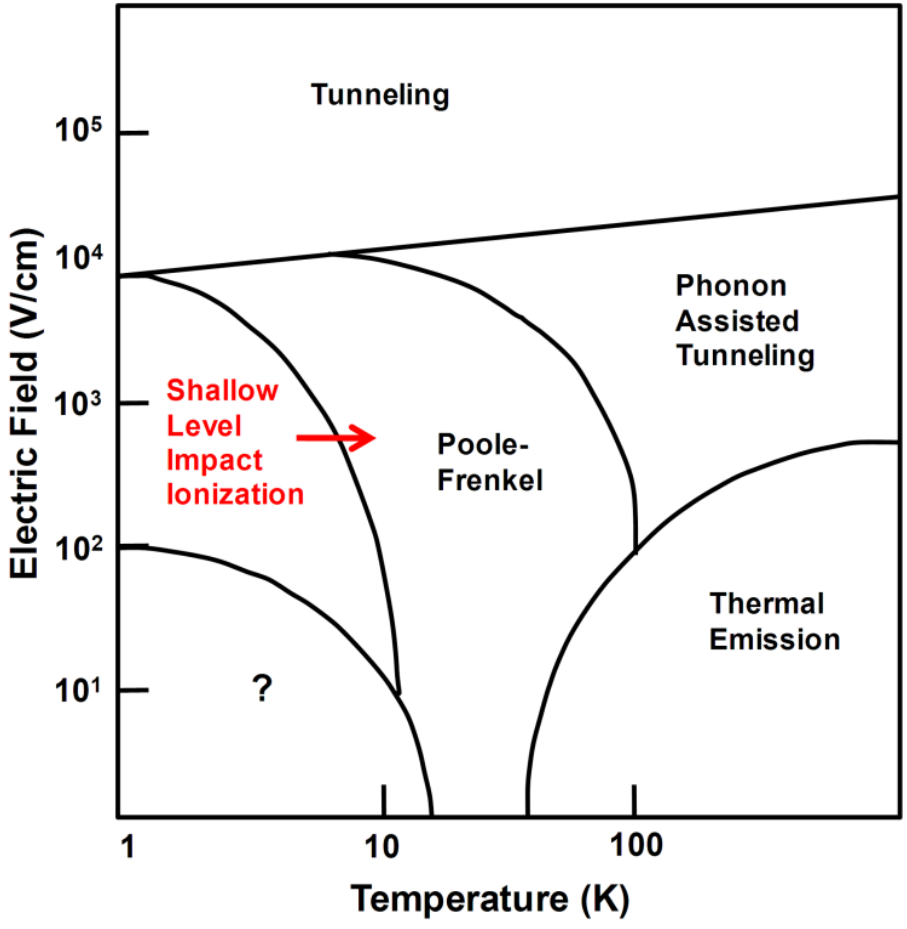


After Simoen et al., "Charge transport in a Si resistor at liquid –He temperatures," JAP 68 (8), 1990.

Dominant Impurity Ionization Mechanisms vs Temperature



- **Shallow-level impact ionization (SLII) is field assisted ionization of frozen-out shallow dopants.**
- **SLII can lead to significant charge multiplication when modest electric field threshold is reached and excess carriers are present**



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Heavy Ion SEL Test Description of 0.5 µm ROIC

- AMI C5 bulk process on lightly doped p-substrate
- ROIC fully functional during testing (4 channels at 500 kHz).
- Four key voltages & associated currents monitored every 25 µs
  - Real time visibility on all supplies
  - V_{pd} (logic portion of readout circuitry) was only supply to latch
- ROIC health monitored throughout the test.

He cryostat in front of TAMU beam line. Five ROICs tested.

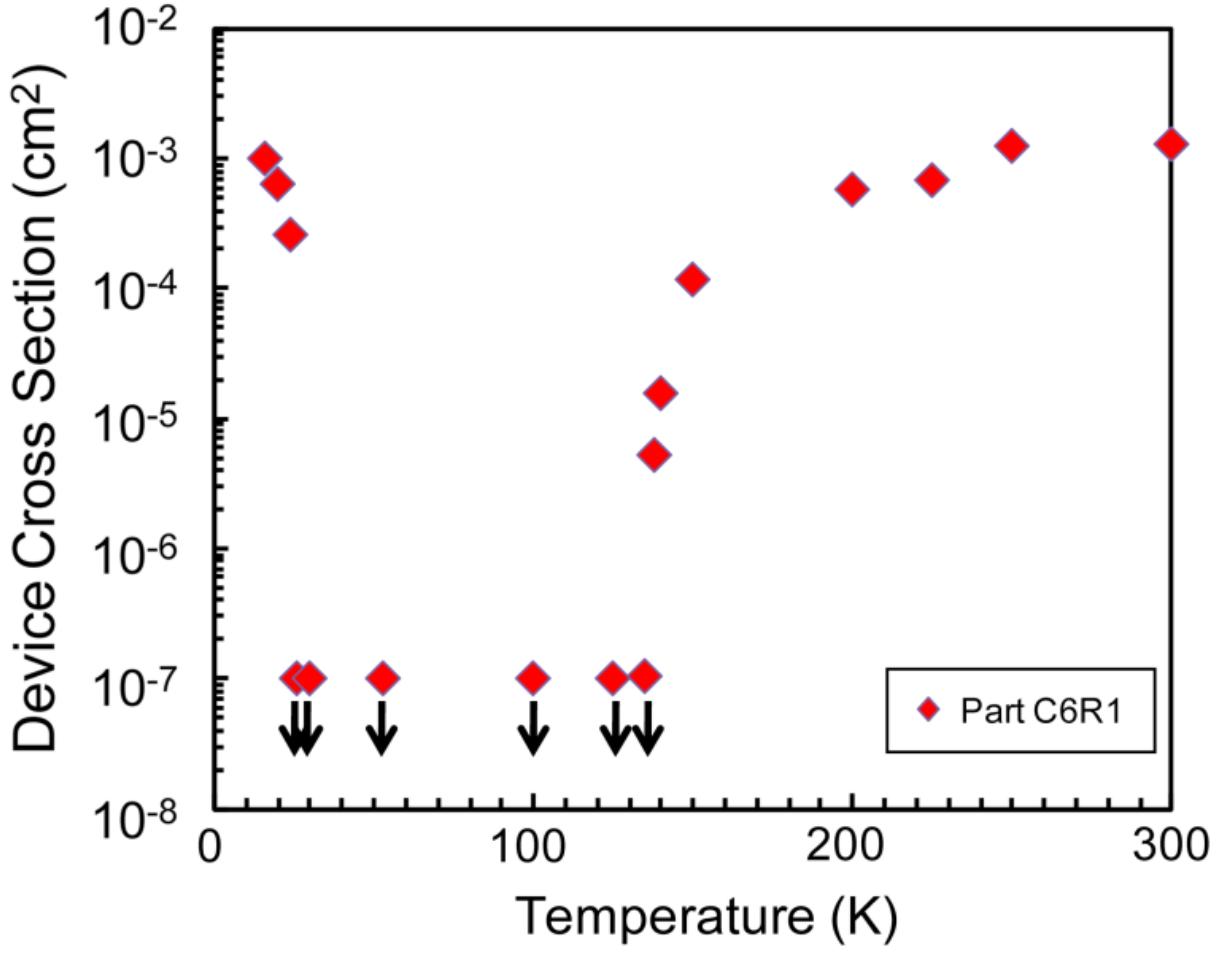
Temperature Dependence of Hard SEL Events

- **Kr ions @ 60º:**

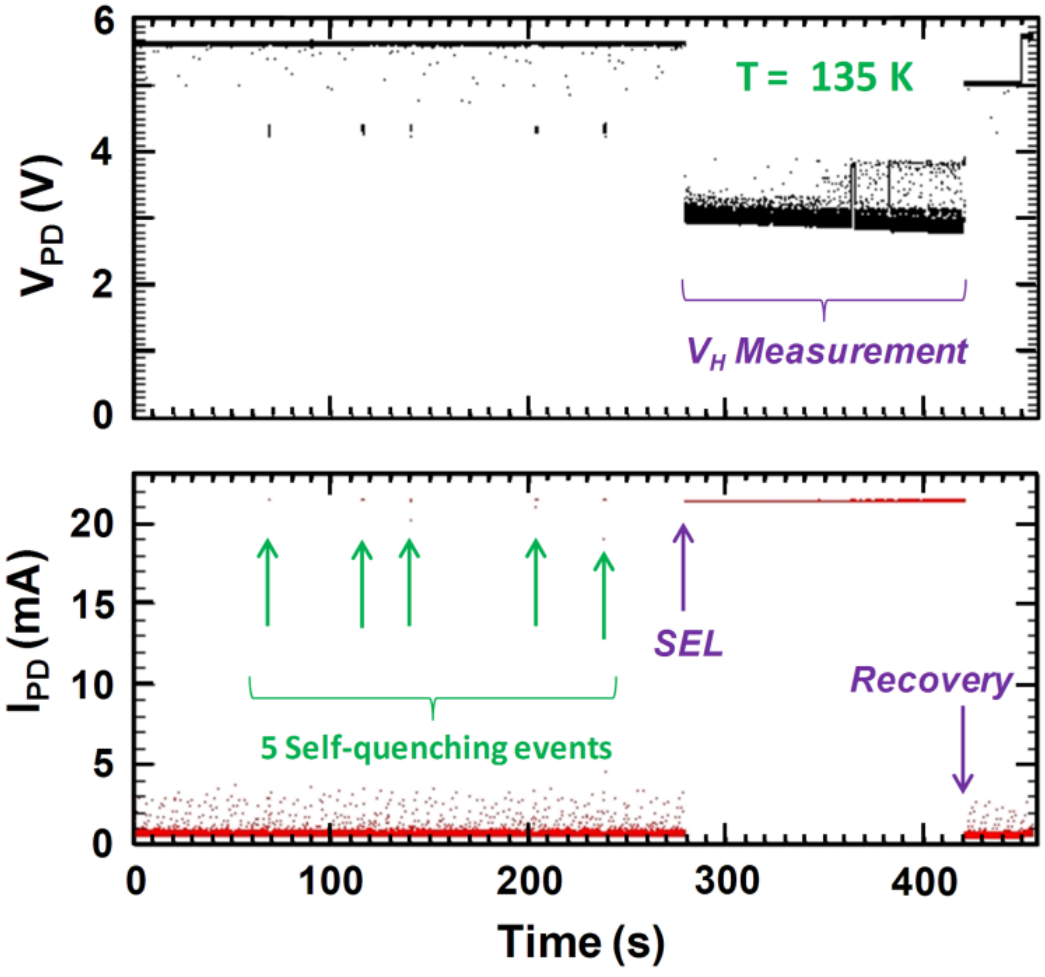
  LET_{eff} = 64 MeVcm²/mg

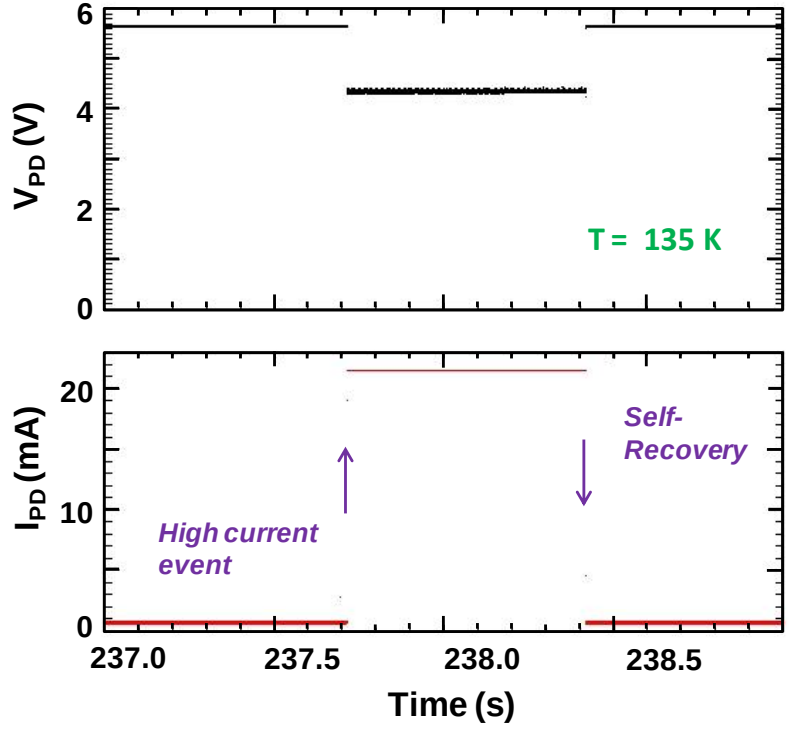
  and R_{proj}= 43 µm

- **Cross sections comparable for 20 K & 300 K**
- **Very modest temperature dependence 200-300 K**
- **Holding voltages (V_H):**
  - **4.1 – 5.6 V (T ≤ 24 K)**
  - **1.9 – 2.8 V (T ≥ 135 K)**
- **Self quenching high current events observed in both transition regions**



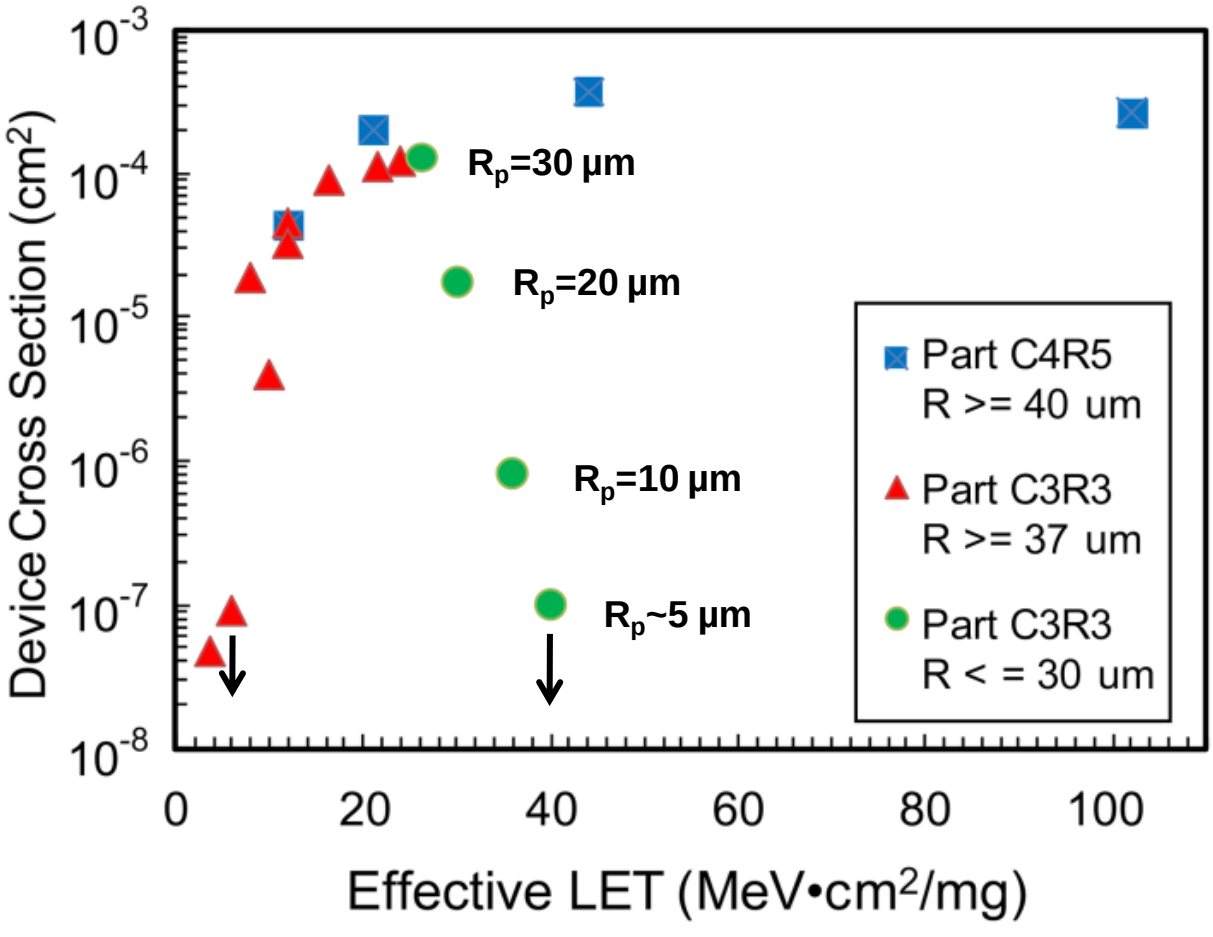
Typical Hard SEL and Self-Quenching High Current Event Signatures





- Holding voltage = 2.8 V
- Note self quenching event had same current level as hard SEL event (~20 mA)

ROIC Latchup Behavior at 20 K



- **Diffusion from substrate is important**
- **No SEL observed for LET_{eff} = 40 & R_p ~4-5 µm!**
  - **Ar-40 ion deposited 28 MeV**
  - **Only self-recovered high current events**
- **Ar-40 ion delivered 80 MeV within 10 µm**
  - **Penetrated the junction region**
  - **Both self-recovered and hard SEL events**

LET_{th}~3.3 at 20 K, but 15 < LET_{th} < 20 at 300 K

'Saturated' cross section 2-3 X higher at 300 K

Shallow-Level Impact Ionization (SLII) Mechanism

- Free carriers produced by ion strike initiates exponential growth in free carriers in internal p- and n-region of parasitic pnpn structure that meet the modest electric field threshold for SLII (E_{th})
- The high V_H we observed are expected for 1st order shallow level impact ionization LU model, and are comparable to those observed by Deferm *et al*.
  - $V_H = 2\ V_{bi} + (E_{th})$ / A-C spacing
  - V_H ~ 4 - 5 V for Deferm *et al*. at 4 - ~50 K
- Our data clearly indicate importance of lightly doped p-substrate
  - SEL cross section reduction striking for R_p < 30 µm at 20 K
  - Slight temperature dependence from 200-300 K
    - Changes in R & V_{BE} with temperature decrease SEL probability
  - Charge collection efficiency may be greater at lower temperatures
    - Longer diffusion length and lower recombination efficiency

Conclusions

- Cryogenic SEL is indeed possible and represents a new qualification concern.
  - Shallow-level impact ionization is a very plausible mechanism to provide a source of carriers below roughly 50 K.
  - NASA requires cryogenic operation for ROICs, ASICs and other CMOS devices for IR sensor applications as well as extreme environments.
- Very little data exists for ion-induced SEL below room temperature
  - We see a significantly lower SEL threshold at 20 K compared to room temperature.
    - 'Saturated' cross section is ~2 - 3 higher at 300 K.
  - Data in the 'classical' regime from 100 – 300 K show SEL behavior beginning at 135 K.
    - Very modest temperature dependence of the SEL cross section from ~200 – 300 K.
      - Similar results for 2nd ROIC on epi from different vendor.
      - 'Test as you fly'